IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems

Oct. 1-3 2014, Amsterdam, The Netherlands

Call for Papers

DFT is an annual Symposium providing an open forum for presentations in the field of defect and fault tolerance in VLSI and nanotechnology systems inclusive of emerging technologies. One of the unique features of this symposium is to combine new academic research with state-of-the-art industrial data, necessary ingredients for significant advances in this field. All aspects of design, manufacturing, test, reliability, and availability that are affected by defects during manufacturing and by faults during system operation are of interest. The topics include (but are not limited to) the following ones:

1. Yield Analysis and Modeling
Defect/Fault analysis and models; statistical yield modeling; critical area and metrics.

2. Testing Techniques
Built-in self-test; delay fault modeling and diagnosis; testing for analog and mixed circuits; signal and clock integrity.

3. Error Detection, Correction, and Recovery
Self-testing and self-checking solutions; error-control coding; fault masking and avoidance; recovery schemes, space/time redundancy; hw/sw techniques.

4. Dependability Analysis and Validation
Fault injection techniques and environments; dependability characterization.

5. Defect and Fault Tolerance
Reliable circuit/system synthesis; radiation hardened/tolerant processes & design; design space exploration for dependable systems, transient/soft faults and errors.

6. Design For Testability in IC Design
FPGA, SoC, NoC, ASIC, microprocessors.

7. Repair, Restructuring and Reconfiguration
Repairable logic; reconfigurable circuit design; DFT for on-line operation; self-healing.

8. Totally Fail-Safe Design for Critical Applications
Methodologies and case study applications to automotive, railway, avionics, industrial control, biomedicine, space and smart power networks.

9. Emerging Technologies
Techniques for CNTs, QCA, DNA, RTDs, SETs, molecular devices and self-assembly.

10. Hardware security
Fault attacks, fault tolerance-based countermeasures, Scan-based attacks and countermeasures, hardware trojans, security vs reliability trade-offs, interaction between VLSI test, trust, and reliability

Paper Submission: Prospective authors are invited to submit original and unpublished contributions (6 pages - with the opportunity to purchase 2 additional ones - in the IEEE conference template, 2-columns style, available on conference web site), to be submitted as PDF file, electronically. Please refer to the symposium web page for updated information:

http://www.dfts.org

We are also interested in panel sessions that involve industrial experiences: please send an email to the Program co-Chairs with a brief description (1 page max) of the proposed panel.

Paper Publication and Author Registration: Only original, unpublished work will be accepted, for regular or poster presentation at the symposium. Proceedings will be published by the IEEE Computer Society and will appear in the Digital Library.

Every accepted paper MUST have at least one *full* paid registration by the time the camera-ready paper is submitted for inclusion in the proceedings, and the author is expected to attend the Symposium and present the paper.

Best Student Paper Award: All papers with a student as both primary author and presenter will be taken into consideration for the 2014 Best Student Paper Award.

Prospective authors should adhere to the following deadlines:

Submission deadline:	**~~9th May, 2014~~** **23 May, 2014**
Notification of acceptance:	**20th June, 2014**
Camera ready full papers:	**25th July, 2014**

For general information, contact the General co-Chairs. For paper submission information, contact the Program co-Chairs. For all updated information, visit our web page.

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